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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/820,735	03/30/2001	Yojiro Matsueda	109098	4744

25944 7590 02/03/2003

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EXAMINER
KOVALICK, VINCENT E

ART UNIT	PAPER NUMBER
2673	

DATE MAILED: 02/03/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/820,735	MATSUEDA, YOJIRO	
	Examiner	Art Unit	
	Vincent E Kovalick	2673	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 March 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,9,14,17-19,24 and 28* is/are rejected.

7)☒ Claim(s) *8,10-13,15,16,20-23 and 25-27* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *3,9&13* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. This Office Action is in response to Applicant's Patent Application, Serial No. 09/820,735, with a File Date of March 30, 2001.

Claim Rejections - 35 U.S.C. § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Zavracky (USP 6,320,568) taken with McKnight (USP 6,104,367) in view of Furuhashi et al. (USP 5,646,644). Relative to claim 1, Zavracky **teaches** a control system for display panels (col. 1, lines 66-67; col. 2, lines 1-67 and col. 3, lines 1-10). Zavracky further **teaches** a display device, comprising: at least one of a semiconductor and an insulating substrate (col. 1, lines 65-67; col. 2, lines 1-4 and Abstract); it being obvious to a person of ordinary skill in the art at the time of the invention that said substrate would server as the base for the storing and display control sections of the said display device.

Zavracky **does not teach** a storing section that stores a digital data signal to control display; and

a display control section that performs display control on the basis of the digital data signal stored by said storing section; the storing section and display section being provided in each dot which is a minimum unit of display and being arranged on the at least one of a semiconductor and an insulating substrate.

McKnight **teaches** a display system having electrode modulation to alter a state of an electro-optic layer (col. 3, lines 6-67 and col. 4, lines 1-59). McKnight further **teaches** a storing section that stores a digital data signal to control a display (col. 13, lines 33-47 and Fig. 6D) said storing section and display section being provided in each dot which is a minimum unit of display (col. 13, lines 14-47).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to incorporate in the device as taught by Zavracky the feature as taught by McKnight in order to put in place the means to store the digital data for controlling the display.

Zavracky taken with McKnight **does not teach** a display control section that performs display control on the basis of the digital data signal stored by said storing section.

Furuhashi et al. **teaches** a liquid crystal display device (col. 1, lines 43-67 and col. 4, lines 1-18); Furuhashi et al. further **teaches** a display control section that performs display control on the basis of the digital data signal stored by said storing section (col. 5, lines 9-25).

It would have been obvious to a person of ordinary skill in the art at the time of the invention

to incorporate in the device as taught by Zavracky taken with McKnight the feature as taught by Furuhashi et al. in order to put in place the means necessary to accommodate storing digital data signals used to control the display device.

4. Claims 2, 6-7 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zavracky taken with McKnight in view of Furuhashi et al. as applied to claim 1 in item 3 herein above, and further in view of Deering (USP 489,956).

Relative to claim 2, McKnight further **teaches** a storing section configured by at least one storing circuit provided at each of interconnections of a plurality of write lines and a plurality of data lines correspondingly to an array pattern of a dot as a minimum unit of display so that, when a write signal is transmitted through said write line and an image signal as a digital data signal to control display is transmitted through said data line, the image signal is stored (col. 13, lines 33-47 and Fig. 6D); and the storage section and display section being provided in each dot which is a minimum unit of display;

Regarding claim 2, Furuhashi et al. further **teaches** a display control section that performs tonal control using a liquid crystal on the basis of an analog signal converted by said converting section (col. 5, lines 9-25).

Zavracky taken with McKnight in view of Furuhashi et al. **does not teach** a converting section that converts a value based on a value of the image signal stored by said storing section into an analog signal.

Deering **teaches** a high performance graphic system (col. 4, lines 21-67; col. 5, 1-67; col. 6, lines 1-67 and col. 7, lines 1-12). Deering further **teaches** a converting section that converts a value based on a value of the image signal stored by said storing section into an analog signal (col. 15, lines 39-42).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to incorporate in the device as taught by Zavracky taken with McKnight in view of Furuhashi et al. the feature as taught by Deering in order to put in place the means for converting the digital signal resident in the storage section to an analog signal for further processing.

Relative to claims 6-7, Deering further **teaches** said display device wherein said converting section performing conversion into the analog signal at a constant period interval (col. 15, lines 39-42 and 48-53); and a duration that no conversion into the analog signal is made being provided in the constant period (col. 15, lines 43-47).

Regarding claim 17, Furuhashi et al. further **teaches** a liquid crystal driving section having areas corresponding to place values represented by image signals stored in the storing circuits (col. 4, lines 55-67 and col. 5, lines 1-5 and Fig. 5)

5. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Zavracky taken with McKnight in view of Furuhashi et al. an further in view of Deering as applied to claim 2 in item 4 hereinabove, still further in view of Yamazaki et al. (USP 6,326,642)

Regarding claim 3, Zavracky taken with McKnight in view of Furuhashi et al. an further in view of Deering **does not teach** said display device wherein said storing circuit of said storing section being configured by a static circuit.

Yamazaki et al. **teaches** an electro-optical display device and semiconductor memory having thin-film transistors (col. 4, lines 35-67; col. 5, lines 1-67; col. 6, lines 1-67 and col. 7, lines 1-38); Yamazaki et al. further **teaches** said display device wherein said storing circuit of said storing section being configured by a static circuit (col. 4, lines 64-67 and col. 5, lines 1-12).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to incorporate in the device as taught by Zavracky taken with McKnight in view of Furuhashi et al. an further in view of Deering the feature as taught by Yamazaki et al. in order to structure the storage such that if would not need a data refresh capability and that once the data is established in a storage unit, it remains until it is updated with new data.

6. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Zavracky taken with McKnight in view of Furuhashi et al. an further in view of Deering as applied to claim 2 in item 4 hereinabove, still further in view of Ishida et al. (USP 6,498,617).

Regarding claim 4, Zavracky taken with McKnight in view of Furuhashi et al. an further in view of Deering **does not teach** said display device wherein said converting section pulse-width -modulating the value based on the image signal to convert the value into the analog signal.

Ishida et al. **teaches** a pulse-width-modulation circuit (col. 2, lines 42-67; col. 3, lines 1-67; col. 4, lines 1-67 and col. 5, lines 1-24); Ishida et al. further **teaches** said display device wherein

said converting section pulse-width-modulating the value based on the image signal to convert the value into the analog signal (col. 3, lines 4-9).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to incorporate in the device as taught by Zavracky taken with McKnight in view of Furuhashi et al. an further in view of Deering the feature as taught by Ishida et al. in order to incorporate the means to generate an analog signal form a pulse-width-modulated digital signal.

7. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Zavracky taken with McKnight in view of Furuhashi et al. an further in view of Deering as applied to claim 2 in item 4 hereinabove, still further in view of Kougami et al. (USP 6,333,766).

Relative to claim 5, Zavracky taken with McKnight in view of Furuhashi et al. an further in view of Deering **does not teach** said display device wherein said converting section converting the value based on the image signal into the analog signal modulated to a pulse width based on a gamma-characteristic.

Kougami et al. **teaches** a tone display method and apparatus for displaying image signal (col. 2, lines 13-67; col. 3, lines 1-67; col. 4, lines 1-67 and col. 5, lines 1-55); Kougami et al. further **teaches** said display device wherein said converting section converting the value based on the image signal into the analog signal modulated to a pulse width based on a gamma-characteristic (col. 11, lines 29-34).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to incorporate in the device as taught by Zavracky taken with McKnight in view of Furuhashi et al.

an further in view of Deering the feature as taught by Kougami et al. in order to apply gamma correction to the pulse width based digital signal.

8. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Zavracky taken with McKnight in view of Furuhashi et al. an further in view of Deering as applied to claim 6 in item 4 hereinabove, still further in view of Osada et al. (USP 5,973,456).

Regarding claim 9, Zavracky taken with McKnight in view of Furuhashi et al. an further in view of Deering **does not teach** said display device wherein an alternating current drive voltage corresponding to the constant period being applied to said display control section.

Osada et al. **teaches** an electroluminescent display device having uniform display element column luminosity (col. 1, lines 61-67 and col. 2, lines 1-49); Osada et al. further teaches said display device wherein an alternating current drive voltage corresponding to the constant period being applied to said display control section (col. 3, lines 13-22).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to incorporate in the device as taught by Zavracky taken with McKnight in view of Furuhashi et al. an further in view of Deering the feature as taught by Osada. et al. in order to supply the alternating current drive voltage to the display control section at the correct time in a cycle.

9. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Zavracky taken with McKnight in view of Furuhashi et al. an further in view of Deering as applied to claim 2 in item 4 hereinabove, still further in view of Takeuchi (US RE37,879 E).

Relative to claim 18, Zavracky taken with McKnight in view of Furuhashi et al. an further in view of Deering **does not teach** said display device further including a plurality of read lines laid correspondingly to said dot array pattern so that, if a read signal is transmitted, the image signals stored in said storing circuits are read out of said storing section.

Takeuchi **teaches** an image control device for use in a video multiplexing system; Takeuchi further **teaches** said display device further including a plurality of read lines laid correspondingly to said dot array pattern so that, if a read signal is transmitted, the image signals stored in said storing circuits are read out of said storing section (col. 5, lines 43-46).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to incorporate in the device as taught by Zavracky taken with McKnight in view of Furuhashi et al. an further in view of Deering the feature as taught by Takeuchi in order to incorporate the means for transferring the image signal from the storing circuits.

10. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Zavracky taken with McKnight in view of Furuhashi et al. in further view of Deering as applied to claim 2 in item 4 herein above, and further in view of Kimura et al. (USP 6,462,722).

Relative to claim 14, Zavracky taken with McKnight in view of Furuhashi et al. and further in view of Deering **does not teach** current-driven luminescent devices having areas corresponding

to place values represented by image signals stored in said storing circuits; and a display control section provided in each dot to control emission of light of said current-driven luminescent devices.

Kimura et al. **teaches** a current-driven light-emitting display apparatus and method of producing the same (col. 1, lines 30-67 and col. 2, lines 1-14); Kimura et al. further **teaches** current-driven luminescent devices having areas corresponding to place values represented by image signals stored in said storing circuits; and a display control section provided in each dot to control emission of light of said current-driven luminescent devices (col. 10, lines 29-34).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to incorporate in the device as taught by Zavracky taken with McKnight in view of Furuhashi et al. the feature as taught by Kimura et al. in order to put in place the means for controlling the emission of light from the current driven luminescent device.

11. Claims 19, 24 and 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over Zavracky taken with McElroy et al. (USP 4,156,927) in view of Itou (USP 6,104,641) taken with Smith et al. (USP 6,278,428) still further in view of Francis (USP 5,841,411).

Regarding claim 19, Zavracky **teaches** a display device, comprising: at least one of a semiconductor and an insulating substrate (col. 1, lines 65-67; col. 2, lines 1-4 and Abstract); it being obvious to a person of ordinary skill in the art at the time of the invention that said substrate would server as the base for the storing and display drive sections of the said display device;

Zavracky **does not teach** a display drive section having a plurality of word lines, a plurality of write lines and a plurality of data lines laid correspondingly to an array pattern of a dot as a minimum unit of display, and a display control section operating, when at least a write signal is transmitted through said write lines and the image signals are transmitted through said data lines, on the basis of said storing section that stores the image signals, the image signals and a word signal transmitted through said word lines, provided in each of the dot array patterns; a word line driver section that controls transmission of a word signal to said word lines; a row decoder section that selects a row for transmitting a write signal to said write lines, to transmit the write signal to a selected row; a column decoder section that selects said data line; a column selection switch section that transmits the image signals as data signals to control display to said data line selected by said column decoder section;

McElroy et al. **teaches** a digital processor system with direct access memory; McElroy et al. further **teaches** a display drive section (col.4, lines 29-32) having a plurality of word lines (col. 5, lines 63-66), a plurality of write lines (col 14, lines 25-34),and a plurality of data lines (col. 10, lines 7-11) laid correspondingly to an array pattern of a dot as a minimum unit of display, and a display control section operating, when at least a write signal is transmitted through said write lines and the image signals are transmitted through said data lines, on the basis of said storing section that stores the image signals (col. 5, lines 45-66), the image signals and a word signal transmitted through said word lines, provided in each of the dot array patterns;

It would have been obvious to a person of ordinary skill in the art at the time of the invention to incorporate in the device as taught by Zavracky the features as taught by McElroy et al. in order to put in place the means to access the data stored in the storage section.

Zavracky taken with McElroy et al. **does not teach** a word line driver section that controls transmission of a word signal to said word lines; a row decoder section that selects a row for transmitting a write signal to said write lines, to transmit the write signal to a selected row; a column decoder section that selects said data line; a column selection switch section that transmits the image signals as data signals to control display to said data line selected by said column decoder section;

Itou **teaches** a switchable multi bit semiconductor memory device (col. 1, lines 43-67 and col. 2, lines 1-62); Itou further **teaches** a word line driver section that controls transmission of a word signal to said word lines (col. 4, lines 59-65 and Fig. 2).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to incorporate in the device as taught by Zavracky taken with McElroy the feature as taught by Itou in order to put in place the means to control the transmission of a word signal to the word lines.

Zavracky taken with McElroy et al. in view of Itou **does not teach** a row decoder section that selects a row for transmitting a write signal to said write lines, to transmit the write signal to a selected row; a column decoder section that selects said data line; a column selection switch section that transmits the image signals as data signals to control display to said data line selected by said column decoder section.

Smith et al. **teaches** a display panel (col. 2, lines 52-67; col. 3, lines 1-23 and Fig. 6); Smith et al. further **teaches** a row decoder section that selects a row for transmitting a write signal to said write lines, to transmit the write signal to a selected row (col. 5, lines 65-67 and col. 6, lines 1-2 and Fig. 6); and a column decoder section that selects said data line (col. 4, lines 64-65).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to incorporate in the device as taught by Zavracky taken with McElroy in view of Itou the features as taught by Smith et al. in order to put in place the means to transmit the write signal to a selected row and select a desired data line.

Zavracky taken with McElroy in view of Itou taken with Smith et al. **does not teach** a column selection switch section that transmits the image signals as data signals to control display to said data line selected by said column decoder section.

Francis **teaches** an active matrix liquid crystal display device (col. 3, lines 9-67; col. 4, lines 1-67 and col. 5, lines 1-36); Francis further **teaches** a column selection switch section that transmits the image signals as data signals to control display to said data line selected by said column decoder section (col. 6, lines 35-40).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to incorporate in the device as taught by Zavracky taken with McElroy in view of Itou taken with Smith et al. the feature as taught by Francis in order to put in place the means to transmit the image signals as data signals to control display to said data lines.

Relative to claim 24, Smith et al. further **teaches** said display device wherein said row decoder section selecting a row for transmitting the write signal on the basis of an address signal representing a storage position (col. 3, lines 51-63).

Regarding claim 28, Smith et al. further **teaches** said display device further including: a timing controller section that controls at least timing of transmitting the address signal; a memory controller section that controls transmission of the image signals; the timing controller section and the memory controller section being integrated and integrally formed on said at least one of a semiconductor and an insulating substrate (col. 7, lines 40-42).

Allowable Subject Matter

12. Claims 8, 10-13, 15-16, 20-23 and 25-27 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Relative to claim 8, the prior art of record **does not teach** each converting section being different in a start time of the constant period, and the period and the duration no conversion into the analog signal is made being different.

Relative to claim 10, the prior art of record **does not teach** the alternating current drive voltage being a voltage driven at VCOM±Va with respect to a reference voltage VCOM.

Relative to claim 11, the prior art of record **does not teach** the alternating current drive voltage being a voltage alternating-current-inversion-driven by two voltage-applying lines laid correspondingly to said dot array pattern.

Relative to claim 12, the prior art of record **does not teach** a plurality of rows of said dot array being provided by groups, and rows in pair being set in each of the groups to invert a phase of the alternating current drive voltage applied.

Relative to claim 13, the prior art of record **does not teach** said display control section controlling light emission of current-driven luminescent devices in connection on the basis of the analog signal in place of performing tonal control using a liquid crystal, thereby effecting tonal control.

Relative to claim 20, the prior art of record **does not teach** said display device further including a converting section that converts a value based on the image signals stored in said storing section into an analog signal provided in each dot array pattern in said display drive section, and said display control section operates on the basis of the analog signal and the word signal.

Relative to claim 21, the prior art of record **does not teach** said display device wherein said word lines being laid to transmit the word signal to said display control section on two rows.

Relative to claim 22, the prior art of record **does not teach** said display device wherein said word line driver section and said row decoder section being allocated correspondingly to a length of said display drive section in a column direction, and said column decoder section and said

column selection switch section being allocated correspondingly to a length of said display drive section in a row direction.

Relative to claim 23, the prior art of record **does not teach** said display device wherein each column selection switch structuring said column selection switch section being allocated correspondingly to a width of said dot array pattern.

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. .

U. S. Patent No.	6,388,661	Richards
U. S. Patent No.	6,323,867	Nookala et al.
U. S. Patent No.	6,258,606	Kovacs
U. S. Patent No.	6,064,158	Kishita et al.
U. S. Patent No.	5,841,897	Numakura et al.

Responses

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Vincent E. Kovalick** whose telephone number is **(703) 306-3020**. The examiner can normally be reached Monday-Thursday from 9:00 a.m. to 4:00 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Bipin Shalwala**, can be reached at **(703) 305-4938.**

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Inquires

15. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is **(703) 306-0377**.

Vincent E. Kovalick